CLAIMS

What is claimed is:

1. A method for fabricating an organic memory cell comprising:

forming a substrate layer having a surface that acts as a base for an organic memory cell to be created thereupon;

performing a CMP process on the surface;

exposing the post CMP surface to an inorganic acid for shaping a surface depression thereupon;

growing a passive layer within the depression; and

applying an organic acid to a surface of the grown passive layer, such that

a substantially smooth surface texture is obtained.

2. The method of claim 1, further comprising;

forming a dielectric layer over the passive layer;

forming a layer of organic material over the passive layer; and

forming a second layer on the organic material.

3. The method of claim 1, further comprising:

plating the passive layer by an electroless process.

4. The method of claim 3, further comprising:

controlling the plating process by a controller.

5. The method of claim 1, further comprising:

etching a surface protrusion of the passive layer to a post CMP surface level.

6. The method according of claim 1, further comprising:

exposing the post CMP surface to the inorganic acid in several cycles, and

applying the organic acid in several cycles.

7. A system for removing surface irregularities from an electrode layer of an organic memory cell comprising:

means for forming an electrode layer having an electrode surface;

means for creating a void on the electrode surface;

means for growing a passive layer within the void, such that a crest surface of the passive layer protrudes above the electrode surface; and

means for a leveling off the crest surface to a desired level.

8. A system according to claim 7, the electrode surface being a flat surface.

9. A method for planarizing a CMP processed wafer surface comprising:

providing a CMP processed wafer having an initial surface with micro scratches;

exposing the initial surface to an inorganic acid for shaping a void thereupon;

growing a passive layer within the void, such that a surface of the passive layer forms a protrusion out of the void, extending beyond the initial surface; and

exposing the passive layer to an organic acid.

10. The method of claim 9, further comprising:

selectively depositing an activation compound over the void;

applying a chemical solution to the activation compound as to initiate an electroless reaction, the chemical solution comprising metal ions as well as a reducing agent; and

reducing the metal ions of the chemical as to plate the passive layer within the void.

11. The method of claim 9, further comprising:

growing a Cu_2S, or a CuS or a Cu layer.

12. The method of claim 10, further comprising:

employing at least one of a $CuSO_4$ and a $ZnSO_4$. in the chemical solution.

13. The method of claim 10, further comprising:

controlling the growing of the passive layer within the void.

14. The method of claim 10, further comprising:

depositing SnPd as the activation compound.

15. A method for fabricating a memory cell comprising:

forming a substrate layer having a surface that acts as a base for a memory cell to be created thereupon;

performing a CMP process on the surface;

exposing the post CMP surface to an inorganic acid for shaping a surface depression thereupon;

growing a passive layer within the depression; and

applying an organic acid to a surface of the grown passive layer, such that

a substantially smooth surface texture is obtained.

fabricating an organic memory device having:

a first layer and a second layer comprising an organic layer formed therein, the second layer placed over the first layer; and,

a conductive layer being formed over the organic layer and operative with the first layer to activate a memory portion formed in the organic layer.

16. The method of claim 15 further comprising, applying an organic acid to the surface of the grown passive layer, as to flatten the surface.

17. The method of claim 15 further comprising fabricating the first layer from at least one of a conductive and a semiconductive material.

18. The method of claim 15, further comprising fabricating the passive layer *via* a Cu/ Cu_2S formation.

19. The method of claim 15, further comprising fabricating the organic memory cell such that the second layer is in contact with the first layer.

20. The method of claim 15, further comprising fabricating the organic memory cell such the organic layer in contact with the conductive layer.